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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/805,113

03/19/2004

Neil G. Jacobson

X-1550 US

8497

24309

7590

01/30/2009

XILINX, INC

ATTN: LEGAL DEPARTMENT

2100 LOGIC DR

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EXAMINER

ABAD, FARLEY J

ART UNIT

PAPER NUMBER

2181

MAIL DATE

DELIVERY MODE

01/30/2009

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<p align="center"><b>Advisory Action</b> <b>Before the Filing of an Appeal Brief</b></p>	<p><b>Application No.</b> 10/805,113</p>	<p><b>Applicant(s)</b> JACOBSON ET AL.</p>	
	<p><b>Examiner</b> FARLEY J. ABAD</p>	<p><b>Art Unit</b> 2181</p>	

**--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

THE REPLY FILED 09 January 2009 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

- a) ☐ The period for reply expires \_\_\_\_\_ months from the mailing date of the final rejection.  
b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on \_\_\_\_\_. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

#### AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because  
(a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);  
(b) ☐ They raise the issue of new matter (see NOTE below);  
(c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or  
(d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: \_\_\_\_\_. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).  
5. ☐ Applicant's reply has overcome the following rejection(s): \_\_\_\_\_.  
6. ☐ Newly proposed or amended claim(s) \_\_\_\_\_ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).  
7. ☐ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.  
The status of the claim(s) is (or will be) as follows:  
Claim(s) allowed: \_\_\_\_\_.  
Claim(s) objected to: \_\_\_\_\_.  
Claim(s) rejected: \_\_\_\_\_.  
Claim(s) withdrawn from consideration: \_\_\_\_\_.

#### AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).  
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).  
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

#### REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because:  
See Continuation Sheet.  
12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). \_\_\_\_\_.  
13. ☐ Other: \_\_\_\_\_.

/Alford W. Kindred/  
Supervisory Patent Examiner, Art Unit 2181

Continuation of 11. does NOT place the application in condition for allowance because: Applicant's arguments are not persuasive and therefore the Examiner respectfully disagrees with these arguments. Lulla discloses a plurality of devices such as bits of memory (metal options), look-up table, ROM EPROM. It is well known in the art that metal option circuits are in fact devices. Given the definition of "device," which is a thing made for a particular purpose, metal option circuits are just that. Geer discloses a plurality of devices arranged and coupled in a scan chain, and generating the system identifier value as a function of positions of the plurality of devices in a scan chain [col. 5, lines 29-35]. The chip ID or level ID SRLs indicate the position of the SRLs to retrieve the ID number. Claim 1 simply states, generating the first system identifier value is further a function of respective positions of the first plurality of devices in a scan chain, nothing more. Geer discloses "the chip ID or level ID SRLs indicating location of the SRLs to retrieve the stored identification number." Aralis discloses storing and reading identification codes from a plurality of devices coupled in a scan chain [figs. 1 and 4, col. 3, lines 60-68, col. 4, lines 12-21, col. 7, lines 49-55]. Furthermore, Aralis discloses generating a system identifier as a result of the read values [col. 4, lines 26-32]. Aralis discloses comparing and configuring as recited in claim 1 as well [col. 4, lines 38-55]. 1. In response to applicant's argument that Aralis has no need for the single target system identifier value generated as a function of all the values read from the plurality of devices, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, combining Geer with the cited references would facilitate efficient and reliable chip identification [col. 2, lines 14-18]. Combining Aralis with the cited references would avoid or minimize reconfiguration [col. 1, lines 42-50].